

REMARKS

Claims 1-15 are pending in the application. Claims 1-15 are rejected.

The drawings were objected. In the attached proposed drawing correction, the drawings have been corrected, as shown by red ink markings on Figures 1 and 2.

The claims were rejected under 35 U.S.C. 112, second paragraph. Referring to Figure 2, the diode of the claims is diode connected transistor Q0, the first transistor is transistor Q1, the first resistor is resistor R4, the second transistor is transistor Q2, the second resistor is resistor R2, and the voltage supply node is Vcc. Therefore, the claims are believed to be allowable under 35 U.S.C. 112, second paragraph.

Claims 1-3, 6-11, 14, and 15 were rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art. Claims 4, 5, 12, and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art. The admitted prior art does not show, teach, or suggest the diode or the second resistor. Therefore, it is believed that the claims are allowable over the references of record.

It is believed that the above remarks in view of the amendments made in this application are fully responsive to the Official Action. Reconsideration and allowance are therefore respectfully requested.

Respectfully submitted,

A handwritten signature in cursive script, appearing to read "Alan Stewart".

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